

BIPOLAR ANALOG INTEGRATED CIRCUIT

 μ PC1225H

30-50 W POWER AMPLIFIER DRIVER

T-74-05-C1

DESCRIPTION

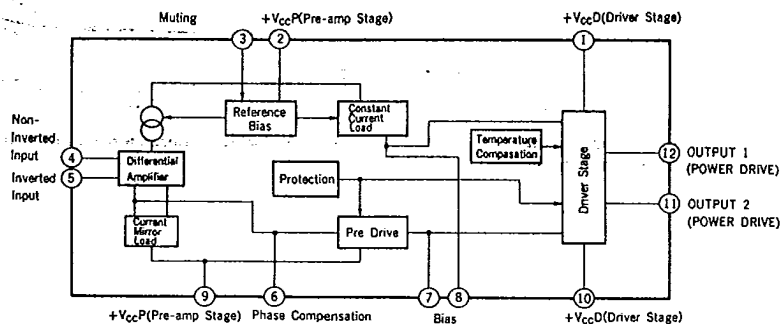
μ PC1225H is designed for use with a HI-FI power amplifier driver. It is composed of a differential amplifier, a pre driver, a driver and protection circuit.

It is in a 12 pin small power SIP. (Single In Line)

FEATURES

- Excellent Low Distortion
0.002 % TYP. ($V_{CC} = \pm 36$ V, $f = 1$ kHz, $A_v = 30$ dB, $P_o = 30$ W, $R_L = 8$ Ohms)
0.006 % TYP. ($V_{CC} = \pm 36$ V, $f = 20$ kHz, $A_v = 30$ dB, $P_o = 30$ W, $R_L = 8$ Ohms)
- Wide Frequency Band
900 kHz TYP. (-3 dB)
- Wide Power Band Width
90 kHz TYP. ($P_o = 25$ W, T.H.D. = 0.1 %)
- Excellent Low POP ON/OFF Noise

BLOCK DIAGRAM



NOTE: The protection circuit is for this IC and cannot protect external Power Transistors. Thus, design a P_o Tr protection circuit besides.

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ABSOLUTE MAXIMUM RATINGS ($T_a = 25^\circ\text{C}$)

Supply Voltage (Quiescent)	V_{CC1}	± 50	V
Supply Voltage (Operational)	V_{CC2}	± 45	V
Quiescent Circuit Current	I_{CC}	200	mA
Allowable Package Dissipation	$I_{CC}(\text{PEAK})$	4.1	W
Operational Temperature	T_{opt}	-20 to +75	$^\circ\text{C}$
Storage Temperature	T_{stg}	-40 to +150	$^\circ\text{C}$

RECOMMENDED OPERATING CONDITION

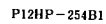
Supply Voltage (Operational)	$V_{CC} = \pm 18$ to ± 36 V at Max Power Output
Input Bias Resistance	$R_{IN} = 1$ to 50 to 100 kohms
Power Transistor h_{FE}	$h_{FE} = 50$ at Max Power Output
Closed Loop Voltage Gain	$A_V = 26$ to 30 dB

ELECTRICAL CHARACTERISTICS ($V_{CC} = \pm 36$ V, $A_V = 30$ dB, Use Standard Test Circuit, $T_a = 25^\circ\text{C}$)

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITION
Output Offset Voltage	V_{OFF}		± 5	± 100	mV	SEE TEST CIRCUIT 1
Quiescent Circuit Current	I_{CC}		20	40	mA	$V_{IN} = 0$
Maximum Output Voltage	V_{OM}	20	23		V	T.H.D. = 0.05 % $f = 20$ to 20 kHz
Open Loop Voltage Gain	A_{VO}	80	95		dB	$V_O = 1.5$ V, $f = 1$ kHz
Output Noise Voltage	V_{NO}		0.07	0.14	mV	$R_G = 10$ kohms
Power Band Width	P.B.W.		900		kHz	$V_O = 1.5$ V, -3 dB
Supply Voltage Rejection Ratio	S.V.R.	55	70		dB	$R_G = 2$ kohms, $f = 100$ Hz

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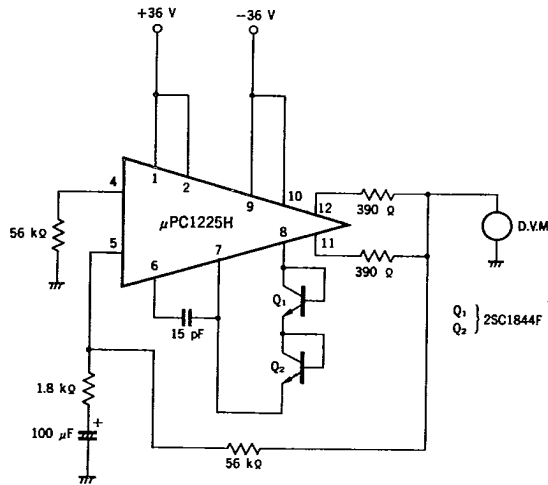
Pin No.	Pin connection
1	+V _{CCD} (for Driver)
2	+V _{CCP} (for Preamp)
3	MUTING
4	INPUT
5	NFB
6	PHASE COMP
7	BIAS
8	BIAS
9	-V _{CCP} (for Preamp)
10	-V _{CCD} (for Driver)
11	LOWER OUTPUT
12	UPPER OUTPUT

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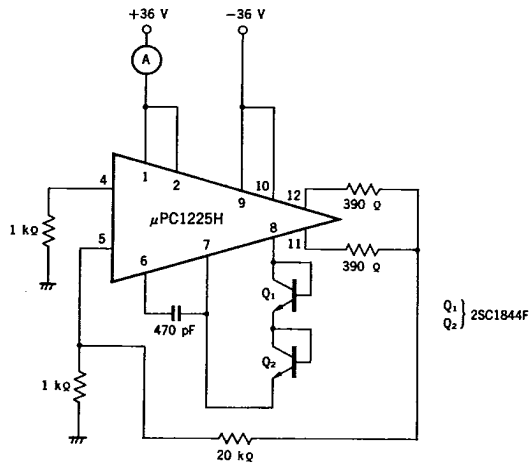
μ PC1225H
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TEST CIRCUIT 1 (V_{OFF})



TEST CIRCUIT 2 (I_{CC})



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μ PC1225H

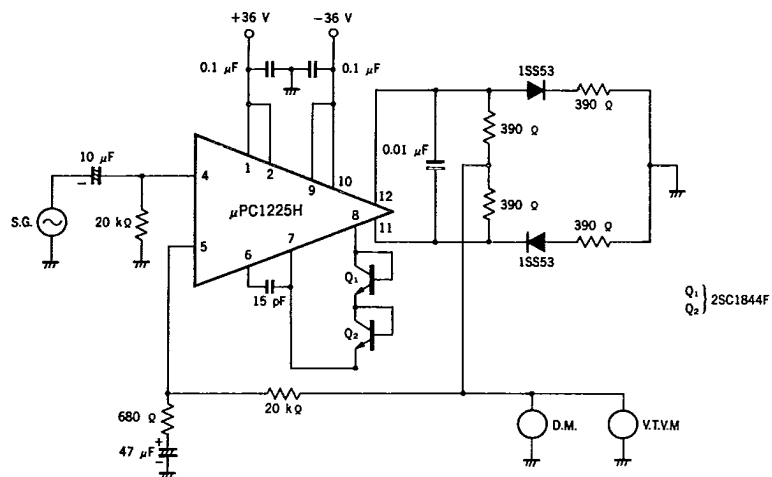
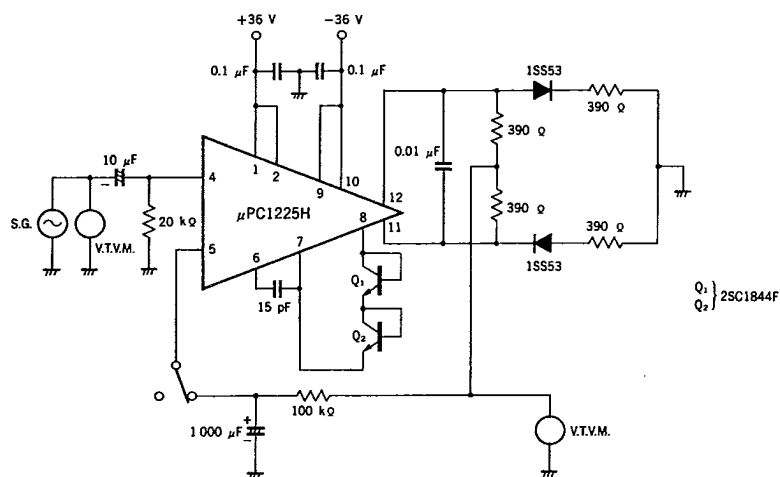
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TEST CIRCUIT 3 (V_{OM})

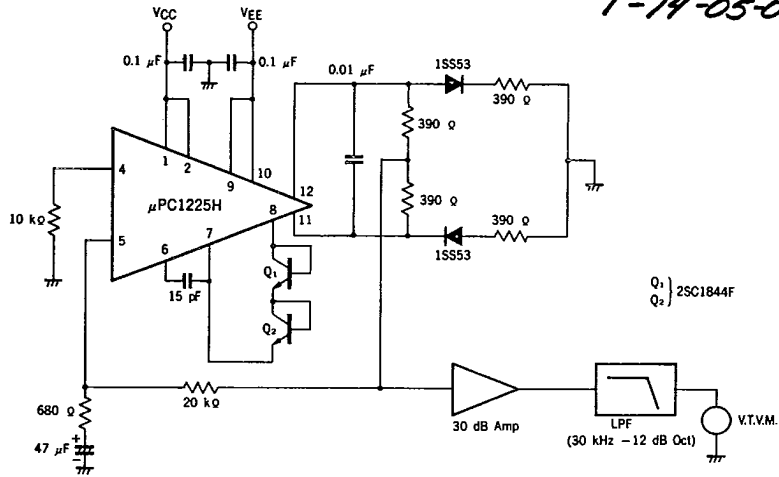
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TEST CIRCUIT 4 (A_{VO})

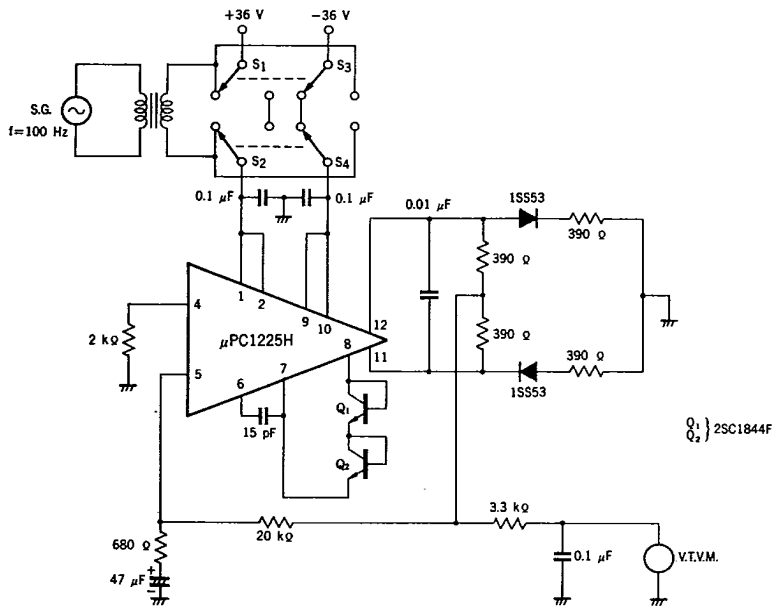
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TEST CIRCUIT 6 (S.V.R.)



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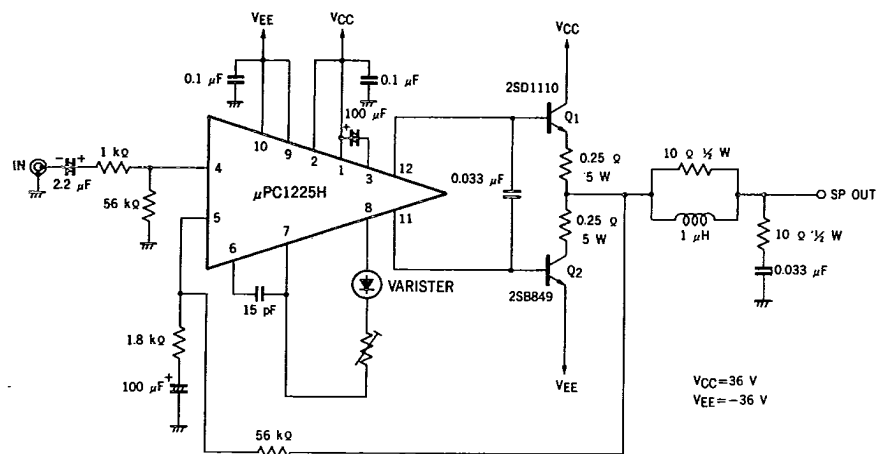
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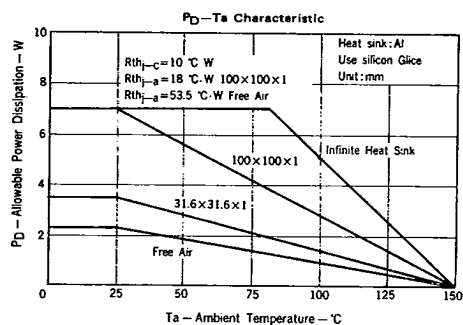
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TYPICAL APPLICATION CIRCUIT



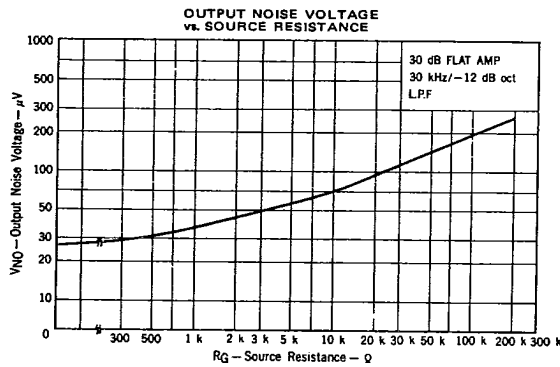
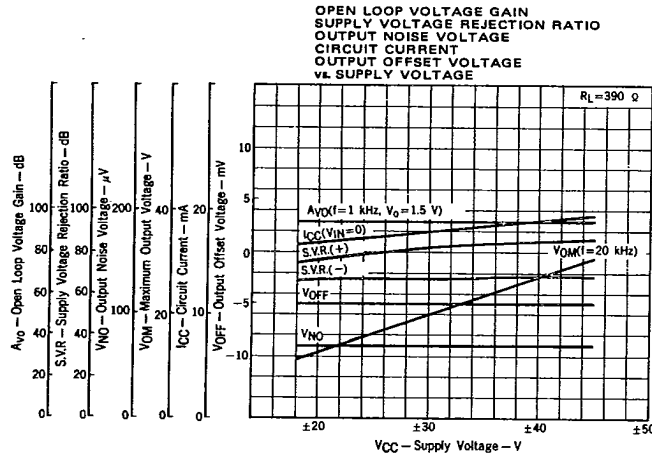
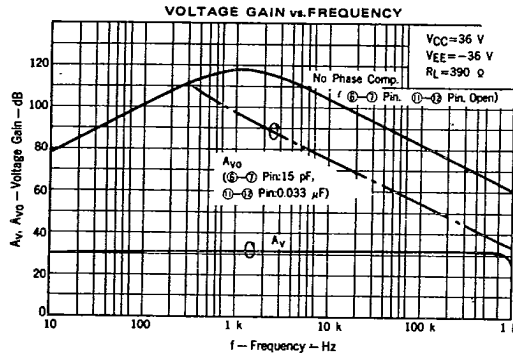
$V_{CC} = 36\text{ V}$
 $V_{EE} = -36\text{ V}$



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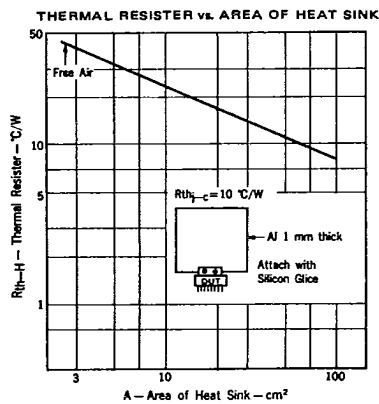
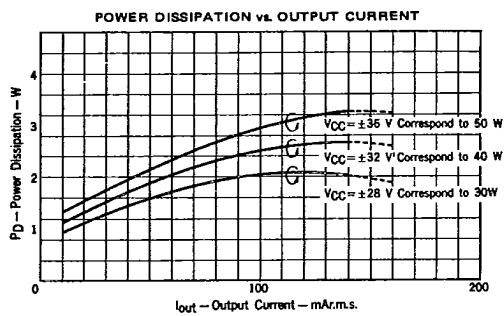
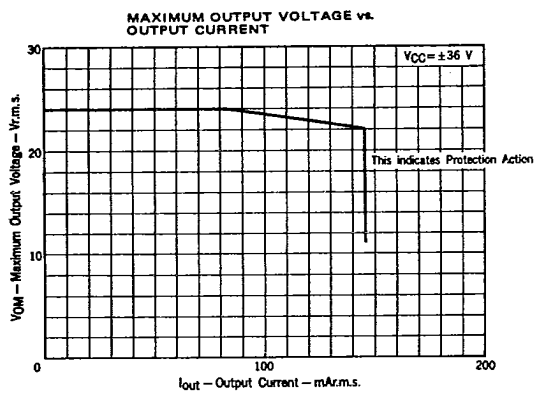
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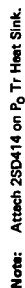
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#12 This indicates a copper board pattern

This is the evaluation circuit. Thus, it is not for a mass production considered about component deviation and the temperature characteristic.

Note:

#1 These terminals are for 3-terminals regulators (μ PC7818H, μ PC7918H) as a μ PC1224H power supply.

#2 These terminals are for JP — lines to a temperature Compensation transistor (2SD414 or others).

#3 Use 0.02 μ F capacitance in case of using μ PC1237H at latching function, while connect each other at automatic resetting.

#4 This capacitance is for preventing POP ON/OFF noise.

Thus, neglect it in case of using a relay.

#5 These terminals are for JP—lines in case of using the same power supply (μPC1237H and Power Amplifier)

#6 These terminals are for JP—lines in case of using the same power supply

#7 This terminal is for AC-OFF Datec-
(μPC1225H and Power Tr)

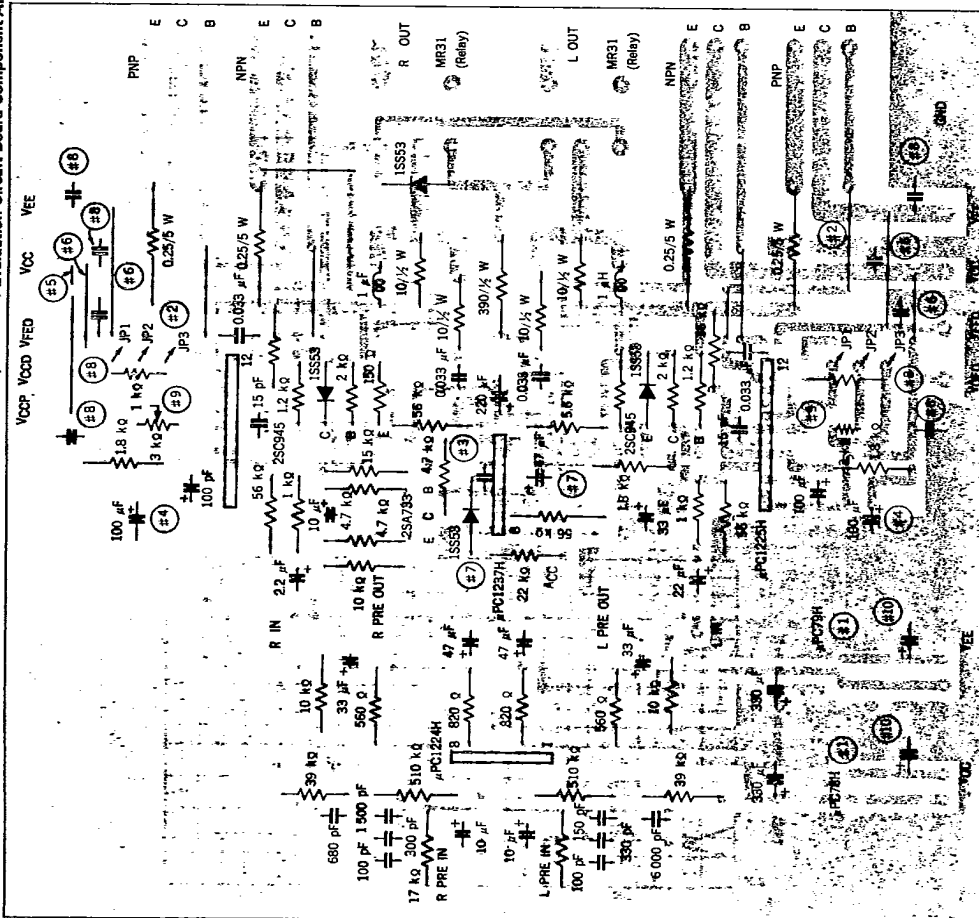
tion. Thus, use 8.2 k ohms instead of 22 k ohms, neglect 1S53 and connect these 1S53's terminals and neglect 4.7 μ F in case of using DC power supply.

#8 These capacitances are for preventing a parasitic oscillation. Use a 0.1 μ F.

#9 These trimmers are for adjusting an idling current. Recommend Neo-Pot PS61 Series.

10 These capacitance are for the 3-terminals regulator input.

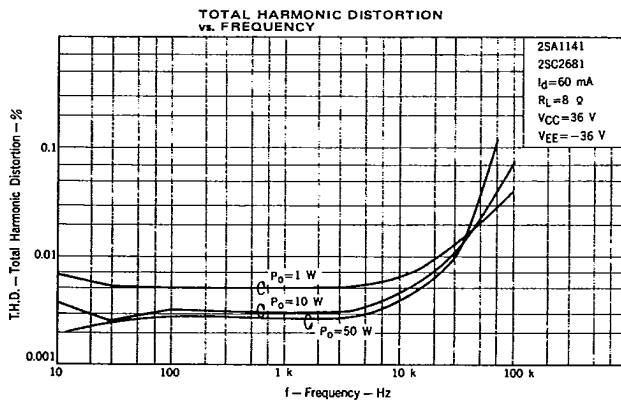
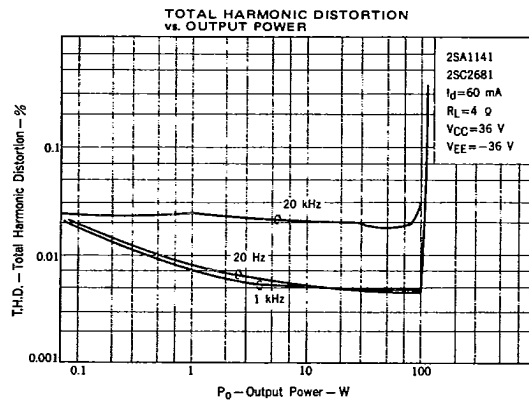
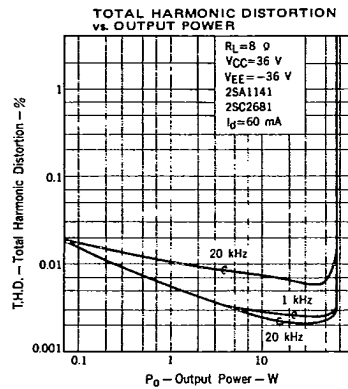
#11 Design of 1 μ H (example)



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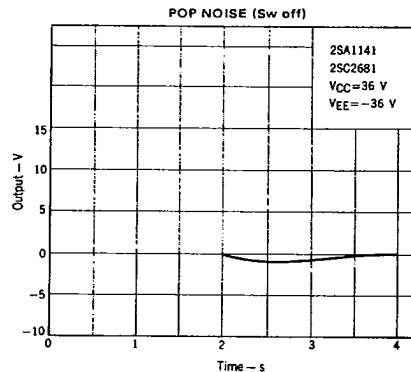
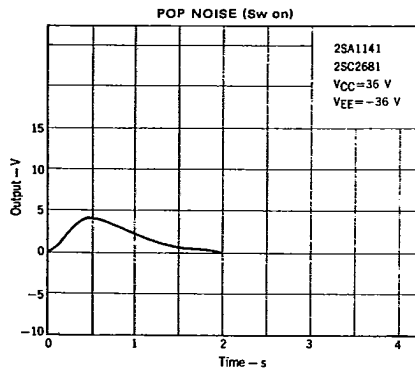
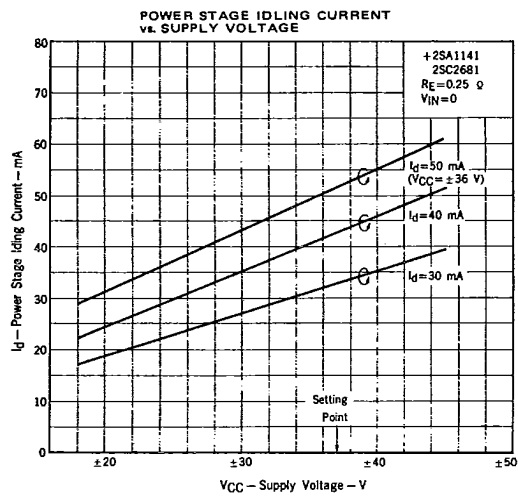
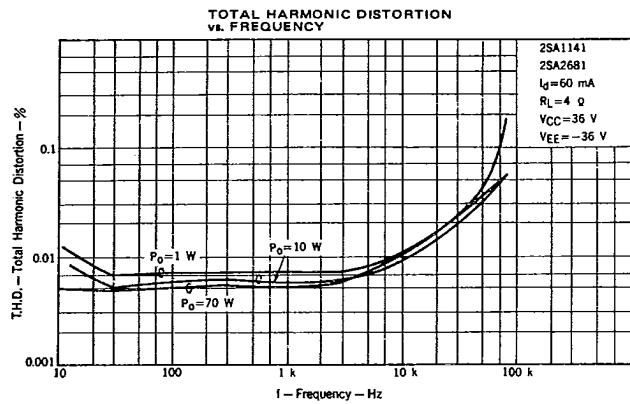
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μ PC1225H

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APPLICATION CIRCUIT

(1) Design Specification

a. Pre amplifier stage (equalizer amplifier)

Supply Voltage $V_{cc} = \pm 22$ VInput equivalent Noise Voltage $V_{NL} = 0.815 \mu V_{r.m.s.}$ TYP.Phono Allowable Input Level 222 mVr.m.s. TYP. (T.H.D.=0.1 %, $f=1$ kHz)

b. Power amplifier stage

Supply Voltage $V_{cc} = \pm 36$ VLoad impedance $R_L = 8 \Omega$ Continuous Output Power $P_o = 50$ W (T.H.D.=0.1 %)Voltage Gain (at flat state) $A_v = 43$ dBInput Sensitivity $V_{in} = 142$ Vr.m.s.Range of Varying Voltage gain 100 Hz ± 10 dB
10 kHz ± 10 dB

(2) Description

μ PC1224H is chosen as EQ amplifier. The internal circuit of this IC is composed of two differential amplifiers as voltage amplifier stage and SEPP output circuit. Thus, this IC is available for flat amplifier and tone control amplifier.

Power amplifier stage is composed of NFB tone control amplifier using μ PC1225H. This power driver IC is also available for flat amplifier. And μ PC1237H is chosen as a protector.

μPC1225H

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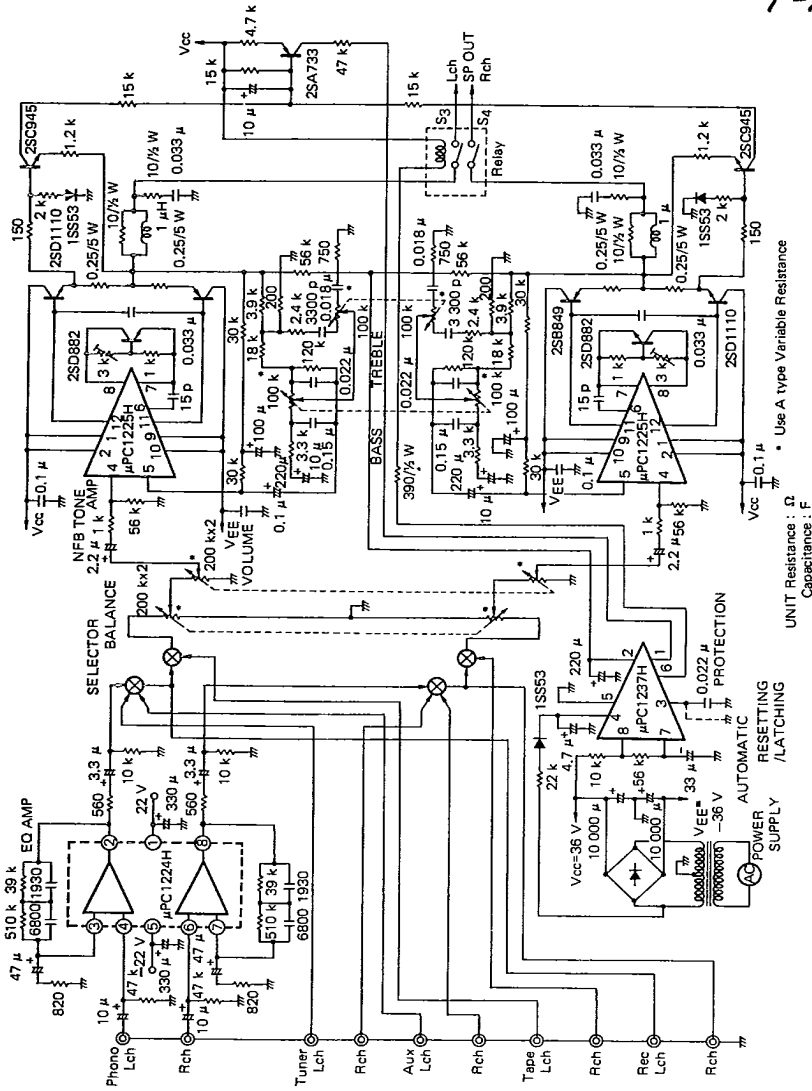


Fig. 1 50 W PRE-MAIN AMPLIFIER APPLICATION CIRCUIT

UNIT Resistance : Ω
Capacitance : F

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(3) Characteristic of Power Amplifier Circuit

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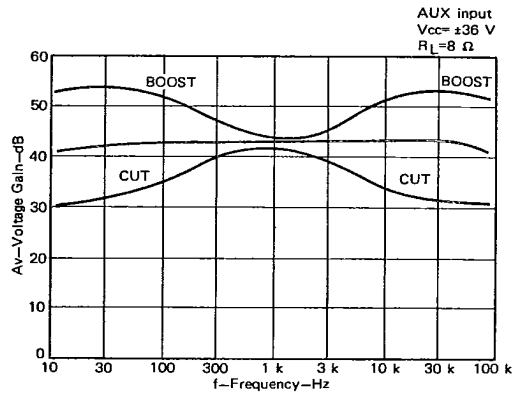


Fig. 2 VOLTAGE GAIN vs. FREQUENCY

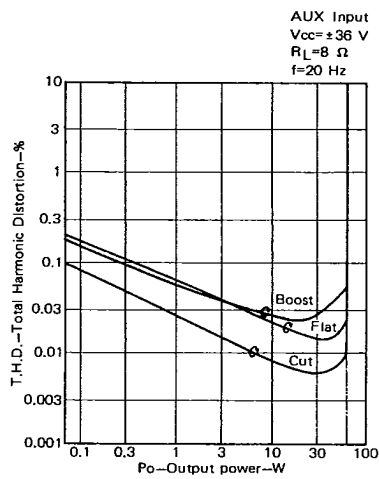


Fig. 3 TOTAL HARMONIC DISTORTION vs. OUTPUT POWER

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μ PC1225H

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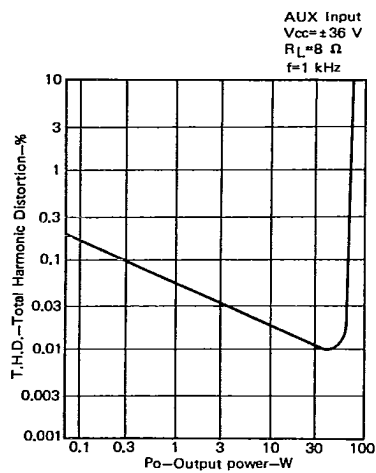


Fig. 4 TOTAL HARMONIC DISTORTION vs. OUTPUT POWER

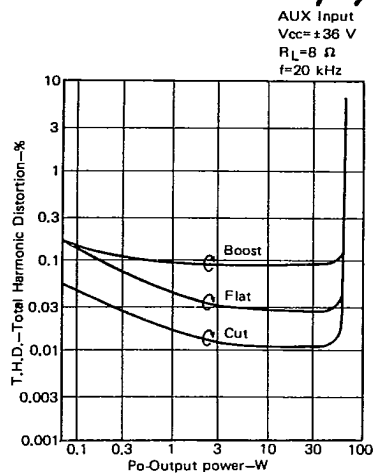


Fig. 5 TOTAL HARMONIC DISTORTION vs. OUTPUT POWER